## ABSTRACT OF THE DISCLOSURE

A processor which decodes and executes an instruction sequence includes: a state hold unit for holding, when a predetermined instruction is executed, a renewal state for an execution result of the predetermined instruction; an obtaining unit for obtaining an instruction sequence composed of instructions matching instructions assigned to an instruction set of the processor, where the instruction set is assigned first conditional instructions, a first state condition for a first conditional instruction being mutually exclusive with a second state condition for a second conditional instruction which has a same operation code as the first conditional instruction, the instruction set not being assigned the second conditional instruction, and the first state condition and the second state condition specifying either of one state and a plurality of states; a decoding unit for decoding each instruction in the obtained instruction sequence one by one; a judging unit for judging whether the renewal state is included in either of the state and the plurality of states specified by the first state condition in the first conditional instruction, when the decoding unit decodes the first conditional instruction; and an execution unit for

executing, only if a judgement result by the judging unit is affirmative, an operation specified by the operation code in the first conditional instruction decoded by the decoding unit.